ACADEMIC REGULATIONS

COURSE STRUCTURE AND DETAILED SYLLABUS

(CHOICE BASED CREDIT SYSTEM (CBCS))

MASTER OF TECHNOLOGY

IN

VLSI SYSTEM DESIGN

For

M.TECH - Regular Two Year Post Graduate Degree Programme

(Applicable for the batches admitted from 2017 - 2018)

DEPARTMENT OF ELECTRONICS AND COMMUINATION ENGINEERING

CMR INSTITUTE OF TECHNOLOGY

(UGC - Autonomous)

Approved by AICTE, Permanently Affiliated to JNTUH & Accredited by NBA

Kandlakoya(V), Medchal (M), Ranga Reddy (DisT.), Hyderabad-501 401, Telangana State

Landline: 08418-200720; Fax: 08418-200240

E-mail: principalcmrit@gmail.com **Web:** www.cmritonline.ac.in

FOREWORD

CMR Institute of Technology, established in the year 2005 has been bestowed with autonomous status by the UGC from the academic year 2017-18 for its remarkable academic accomplishments accompanied by its unflinching spirit and dedication to impart quality technical education to the deserving aspirants. The institution has commenced functioning independently within the set norms prescribed by UGC and AICTE. The performance of the institution manifests the confidence that the prestigious monitoring body, the UGC has on it, in terms of upholding its spirit and sustenance of the expected standards of functioning on its own consequently facilitating the award of degrees for its students. Thus, an autonomous institution is provided with the necessary freedom to have its own **curriculum, examination system and monitoring mechanism**, independent of the affiliating University but under its observance.

CMR Institute of Technology takes pride for having won the confidence of such distinguished academic bodies meant for monitoring the quality in technology education. Besides, the institution is delighted to sustain the same spirit of discharging the responsibilities that it has been conveying since a decade to attain the current academic excellence, if not improving upon the standards and ethics. Consequently, statutory bodies such as the Academic Council and the Boards of Studies have been constituted under the supervision of the Governing Body of the college and with the recommendations of the JNTU Hyderabad, to frame the regulations, course structure and syllabi for autonomous status.

The autonomous regulations, course structure and syllabi have been framed in accordance with the vision and mission of the institution along with certain valuable suggestions from professionals of various ancillary fields such as the academics, the industry and the research, all with a noble vision to impart quality technical education and contribute in catering full-fledged engineering graduates to the society.

All the faculty members, the parents and the students are requested to study all the rules and regulations carefully and approach the Principal to seek any clarifications, if needed, without presumptions, to avoid unwanted subsequent inconveniences and embarrassments. The cooperation of all the stake holders is sought for the successful implementation of the autonomous system in the larger interests of the institution and for brightening the career prospects of engineering graduates.

PRINCIPAL

CMR INSTITUTE OF TECHNOLOGY

Vision: To create world class technocrats for societal needs.

Mission: Impart global quality technical education for a better future by providing appropriate learning environment through continuous improvement and customization.

Quality Policy: Strive for global excellence in academics & research to the satisfaction of students and stakeholders.

Department of ECE

Vision:

To be a centre of excellence in education and research in Electronics and Communication Engineering

Mission:

- Impart fundamentals along with theoretical and experimental knowledge through cutting edge technologies for career advancement and research.
- Inculcate self learning ability, human values, professional ethics and team building skills to serve the society.
- Foster regular interaction with various stakeholders for holistic development.

M.Tech. - Regular Two Year Post Graduate Degree Programme
(For batches admitted from the academic year 2017 - 18)

PREAMBLE

For pursuing M.Tech. - Regular Two Year Post Graduate Degree Programme offered by **CMR Institute of Technology (CMRIT)** under Autonomous status will herein be referred to as CMRIT (Autonomous).

All the specified rules are herein approved by the Academic Council. These rules will be in force and are applicable to students admitted from the academic year 2017-18 onwards. Any reference to "**Institute**" or "**College**" in these rules and regulations stand for CMRIT (Autonomous).

All the rules and regulations specified shall hereafter be read as a whole for the purpose of interpretation, as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, CMRIT (Autonomous) shall be The Chairman, Academic Council.

1. POST GRADUATE PROGRAMS OFFERED

CMR Institute of Technology, an autonomous college affiliated to JNTUH, offers M.Tech. - Regular 2 years (4 semesters) Post Graduate Degree Programme, under Choice Based Credit System (CBCS) with effect from the academic year 2017 - 18 onwards. The following specializations are offered at present for the M. Tech. programme of study.

Sl. No.	Programme	Offering Department
1	Structural Engineering	Civil Engineering
2	CAD/CAM	Mechanical Engineering
3	VLSI System Design	Electronics & Communication Engineering
4	Computer Science and Engineering	Computer Science and Engineering

2. ADMISSION CRITERIA AND MEDIUM OF INSTRUCTION

2.1. Admission into first year of M.Tech. - Regular Two Year Post Graduate Degree Programme

2.1.1 Eligibility: A candidate seeking admission into the first year of M.Tech. shall be made subject to eligibility and qualification as prescribed by the university from time to time. Admissions shall be made on the basis of merit/rank obtained by the candidate qualified at TSPGECET/GATE or any entrance test conducted by the university or on the basis of any other order of merit as approved by the university, subject to reservations as laid down from time to time by government of Telangana.

2.1.2 Admission Procedure: Admissions are made into the first year M.Tech. as per the stipulations of the TSPGECET/GATE.

(a) Category A: 70% seats are filled through TSPGECET/GATE counselling.
(b) Category B: 30% seats are filled by the management.

2.2. College Transfers: There shall be no college transfers after the completion of admission process.

2.3. Medium of Instruction: The medium of instruction and examinations for the entire M.Tech. - Programme will be in **English** only.

3. M.Tech. PROGRAMME STRUCTURE

3.1 Admitted under M.Tech. - Regular Two Year Post Graduate Degree Programme:

3.1.1 A student after securing admission shall pursue the post graduate programme in M.Tech. Programme for a minimum period of two academic years (4 semesters), and a maximum period of four academic years (8 semesters) starting from the date of commencement of first year first semester. However, he is permitted to write the examinations for two more years after four academic years of course work, failing which he shall forfeit his seat in M.Tech. Programme.

3.1.2 Each semester of I year are structured to provide 28 credits and each semester of II year are structured to provide 16 credits totaling to 88 credits for the entire M.Tech. Programme.

3.1.3 Each student shall secure 88 credits (with CGPA ≥ 5) required for the completion of the post graduate programme and award of the M.Tech. degree.

3.2 **UGC/AICTE** specified definitions/ descriptions are adopted appropriately for various terms and abbreviations used in these academic regulations/ norms, which are listed below.

3.2.1 Semester Scheme:

M.Tech. (Regular) Programme is of 2 academic years (4 semesters) with the academic year being divided into two semesters of 22 weeks (≥ 90 instructional days) each, each semester having - 'Continuous Internal Evaluation (CIE)' and 'Semester End Examination (SEE)', Choice Based Credit System (CBCS) and Credit Based Semester System (CBSS) as indicated by UGC and curriculum/course structure as suggested by AICTE / JNTUH.

3.2.2 Credit Courses:

a) All subjects/courses are to be registered by a student in a semester to earn credits. Credits shall be assigned to each subject/course in a L : P : C (Lecture Periods: Practical Periods : Credits) structure, based on the following general pattern.

- One Credit - for One hour/Week/Semester for Theory/Lecture (L) Courses; and
- One Credit - for Two hours/Week/Semester for Laboratory/Practical (P) Courses

b) **Contact Hours:** Weekly contact hours - equal to 32 hours per week (i.e. 1 hour = 60 Minutes); for this an average course load of 28 credits per semester in first year and 16 credits per semester in second year.

4. COURSE REGISTRATION

4.1 A **'Faculty Advisor or Counsellor'** shall be assigned to each students, who advises the student about the M.Tech. Programme, its course structure and curriculum, choice/option for subjects/courses, based on his/her competence, progress, and interest.

4.2 Academic section of the college invites **'registration forms'** from students before the beginning of the semester through online submission, ensuring **'date and time stamping'**. The online registration requests for any '**current semester**' shall be completed **before** the commencement of Semester End Examinations (SEE) of the '**preceding semester**'.

4.3 A student can apply for **online** registration, **only after** obtaining the written approval from his faculty advisor or counselor, which should be submitted to the College Academic Section through the Head of the Department. A copy of it shall be retained with the Head of the Department, the faculty advisor and the student.

4.4 A student may be permitted to register for his/her subjects/course of **choice** with a total of 28 credits per semester of first year (Minimum of 24 credits and Maximum of 32 credits, permitted deviation being± 15%), based on his **progress** and SGPA/CGPA, and completion of the '**pre-requisites'** as indicated for various subjects/courses, in the department course structure and syllabus contents. However, a minimum of 24 credits per semester must be registered to ensure the studentship in any semester.

4.5 Choice for 'additional subjects / courses' to reach the maximum permissible limit of 32 credits (above the typical 28 credit norm) must be clearly indicated, which needs the specific approval and signature of the faculty advisor/counsellor.

4.6 If the student submits ambiguous choices or multiple options or erroneous (incorrect) entries during **online** registration for the subject(s)/course(s) under a given/specified course group/ category as listed in the course structure, only the first mentioned subject/course in that category will be taken into consideration.

4.7 Subject/course options exercised through **online** registration are final and **cannot** be changed or inter-changed; further, alternate choices will not be considered. However, if the subject/course that has already been listed for registration by the Head of the Department in a semester could not be offered due to any unforeseen or unexpected reasons, then the student shall be allowed to have alternate choice - either for a new subject (subject to offering of such a subject), or for another existing subject (subject to availability of seats). Such alternate arrangements will be made by the Head of the Department, with due notification and time-framed schedule, within the **first week** from the commencement of class-work for that semester.

4.8 Dropping of subjects/courses may be permitted, only after obtaining prior approval from the faculty advisor / counselor (subject to retaining a minimum of 24 credits), **'within 15 Days of time'** from the commencement of that semester.

4.9 **Open Electives**: Students have to choose open elective-1 in I year I semester and open elective-2 in I year II semester from the open electives list as per course structure.

4.10 **Core Electives**: Students have to choose two core electives (Core Elective-I and Core Elective-II) in I year I semester and another two core electives (Core Elective-III and Core Elective-IV) in I year II semester from the core electives list as per course structure.

5. SUBJECTS / COURSES TO BE OFFERED

5.1 A Subject/Course may be offered to the Students, **if only** a minimum of 1/3 of students register to the course.

i) More than **one faculty member** may be allotted by the department for offer the **same subject** (lab/practical's may be included with the corresponding theory subject in the same semester) in any semester. However, selection choice for students will be based on '**first come first serve** basis and CGPA criterion' (i.e. the first focus shall be on early **online entry** from the student for registration in that semester, and the second focus, if needed, will be on CGPA of the student).

ii) If more entries for registration of a subject come into picture, then the concerned Head of the Department shall take necessary decision, whether or not to offer such a subject/ course for **two (or multiple) sections**.

6. ATTENDANCE REQUIREMENTS

6.1 A Student shall be eligible to appear for the Semester End Examination (SEE) of any Subject / Course, if he acquires a minimum of 75% of attendance in that Subject / Course for that Semester.

6.2 A Student's Seminar Report and Seminar Presentation shall be eligible for evaluation, only if he ensures a minimum of 75% of his attendance in Seminar Presentation Classes during that Semester.

6.3 Condoning of shortage of attendance up to 10% (65% and above, and below 75%) in each Subject / Course of a Semester may be granted by the College Academic Council on genuine and valid grounds, based on the Student's representation with supporting evidence.

6.4 A stipulated fee per Subject / Course shall be payable towards condoning of shortage of attendance.

6.5 Shortage of Attendance below 65% in any Subject / Course shall in **NO** case be condoned.

6.6 A Student, whose shortage of attendance is not condoned in any Subject(s) / Course (s) or seminar in any Semester, is considered as 'Detained in that Subject(s)/ Course(s)' or seminar, and is not eligible to take Semester End Examination(s) of such Subject(s) (and in case of Seminars, his Seminar Report or Presentation are not eligible for evaluation) in that Semester; and he has to seek Re-registration for those Subject(s) / Course (s) in subsequent Semesters, and attend the same as and when offered.

6.7 A candidate shall put in a minimum required attendance at least three (3) theory subjects in each semester for promoting to next semester. In order to qualify for the award of the MTech Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

6.8 A student shall not be promoted to the next semester unless he satisfies the attendance requirement of the present semester, as applicable. They may seek readmission into that semester when offered next.

6.9 If any candidate fulfills the attendance requirement in the present semester, he shall not be eligible for **readmission into the same class.**

7. ACADEMIC REQUIREMENTS

The following academic requirements have to be satisfied, in addition to the attendance requirements mentioned in item no. 6.

7.1 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to each Subject/ Course, if he secures not less than 40% Marks (28 out of 70 Marks) in the End Semester Examination, and a minimum of 50% of Marks in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together; in terms of Letter Grades, this implies securing B Grade or above in that Subject.

7.2 A Student shall be deemed to have satisfied the Academic Requirements and earned the Credits allotted to - Seminar, and Comprehensive Viva-voce, if he secures not less than 50% of the total Marks to be awarded for each. The Student would be treated as failed, if he - (i) does not attend the Comprehensive Viva-voce as per the schedule given, or (ii) does not present the Seminar as required, or (iii) secures less than 50% of Marks (< 50 Marks) in Seminar/ Comprehensive Viva-voce evaluations. He may reappear for comprehensive viva where it is scheduled again; for seminar, he has to reappear in the next subsequent Semesters, as and when scheduled.

7.3 A Student shall register for all subjects covering 88 Credits as specified and listed in the Course Structure for the chosen M.Tech. Specialization, put up all the attendance and academic requirements for securing 88 Credits obtaining a minimum of B Grade or above in each Subject, and 'earn all 88 Credits securing SGPA $\geq$ 5.0 (in each Semester) and final CGPA (ie, CGPA at the end of M.Tech. Programme) $\geq$ 5.0, to successfully complete the M.Tech. Programme.

7.4 Marks and Letter Grades obtained in all those Subjects covering the above specified 88 credits alone shall be considered for the calculation of final CGPA, which shall be indicated in the Grade Card of II Year II Semester.

7.5 If a student registers for some more 'extra Subjects' (in the parent Department or other Departments/Branches of Engg.) other than those listed Subjects totaling to 88 Credits as specified in the Course Structure, the performances in those 'extra Subjects' (although evaluated and graded using the same procedure as that of the required 88 Credits) will not be taken into account while calculating the SGPA and CGPA. For such 'extra Subjects' registered, % marks and Letter Grade alone will be indicated in the Grade Card, as a performance measure, subject to completion of the Attendance and Academic Requirements as stated in Items 6 and 7.1 – 7.4 above.

7.6 Students who fail to earn 88 Credits as per the specified Course Structure, and as indicated above, within 4 Academic Years from the date of Commencement of their I Year, shall forfeit their seats in M.Tech. Programme and their admissions shall stand cancelled.

7.7 When a student is detained due to shortage of attendance in any subject(s)/seminar in any semester, no Grade Allotment will be done for such Subject(s)/Seminar, and SGPA/ CGPA calculations of that Semester will not include the performance evaluations of such subject(s)/seminar in which he got detained. However, he becomes eligible for re-registration of such subject(s)/seminar (in which he got detained) in the subsequent Semester(s), as and when next offered, with the Academic Regulations of the Batch into which he gets readmitted, by paying the stipulated fees per subject. In all these re-registration cases, the student shall have to secure a fresh set of Internal Marks (CIE) and End Semester Examination Marks (SEE) for performance evaluation in such subject(s), and subsequent SGPA/ CGPA calculations.

7.8 A student eligible to appear in the Semester End Examination (SEE) in any subject, but absent at it or failed (failing to secure B Grade or above), may reappear for that subject at the supplementary examination (SEE) as and when conducted. In such cases, his Internal Marks (CIE) assessed earlier for that Subject/ Course will be carried over, and added to the marks to be obtained in the supplementary examination (SEE), for evaluating his performance in that Subject.

8. EVALUATION - DISTRIBUTION AND WEIGHTAGE OF MARKS

8.1 The performance of a student in each semester shall be evaluated subject-wise / course-wise (irrespective of credits assigned) with a maximum of 100 marks for theory. For all theory subjects/practicals, the distribution shall be 30 marks for CIE, and 70 marks for the SEE, and a letter grade corresponding to the percentage of marks obtained shall be given.

8.2 Evaluation of Theory Subjects / Courses

A) Continuous Internal Evaluation: For each theory subject there shall be two mid-term examinations of 30 marks. Each mid-term examination consists of subjective paper for 25 marks and assignment for 5 marks. The better performance out of these two mid-term examinations shall be taken as the final marks secured by the student. The duration of each mid term examination is for 120 minutes. The first mid-term examination shall be conducted for the first 50% of the syllabus, and the second mid-term examination shall be conducted for the remaining 50% of the syllabus as per the academic calendar.

i) The subjective paper shall contain two parts i.e. Part A and Part B. Part A is compulsory question carries 10 marks for which there may be a 5 sub questions carries two mark each and Part B carries 15 marks for which there will be 3 essay questions with internal choice.

ii) The student should submit first assignment before the commencement of the first mid term examinations, and second assignment before the commencement of the second mid-term examinations.

B) Semester End Examinations: The duration of SEE is 3 hours. The details of the question paper pattern are as follows:

- The end semester examinations will be conducted for 70 marks consisting of two parts viz. i) **Part- A** for 20 marks, ii) **Part - B** for 50 marks.
- Part-A is compulsory question which consists of ten sub-questions (two from each unit) carries 2 marks each.
- Part-B consists of five questions (numbered from 2 to 6) carries 10 marks each. One question from each unit with internal choice (i.e., a or b).

8.3 Evaluation of Practical Subjects/Courses: In any semester, a student has to complete all exercises in each practical/laboratory course and get the record certified by the concerned Head of the Department to be eligible for Semester End Examination. For practical/laboratory Subjects, there shall be a Continuous Internal Evaluation (CIE) during the semester for 30 internal marks and 70 marks for Semester End Examination (SEE).

A) Continuous Internal Evaluation (CIE): Out of the 30 marks, 15 marks are allocated for day-to-day work evaluation and for remaining15 marks - two mid-term examinations of each 15 marks will be conducted by the concerned laboratory teacher for a duration of two hours and the better performance of the two mid-term examinations is taken into account.

B) Semester End Examination (SEE): The SEE for practical Subject / Course shall be conducted at the end of the semester by one Internal and one External Examiners appointed by the Head of the Institution as per the recommendation of the concerned Head of the Department.

8.4 Evaluation of Seminar: The student has to enroll and get approval for seminar on a specialized topic from the concerned Advisor / Counselor in the beginning of respective semester. There shall be two seminar presentations during I year I semester and II semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Departmental Academic Committee consisting of Head of the Department, Supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% of marks to be declared successful. If he fails to fulfill minimum marks, he has to **reappear** during the supplementary examinations.

8.5 Evaluation of Comprehensive Viva: There shall be a comprehensive viva-voce in II year I semester. The comprehensive viva-voce is intended to assess the students' understanding of various subjects he has studied during the M.Tech. course of study. The Head of the Department shall be associated with the conduct of the comprehensive viva-voce through a Committee. The Committee shall consist of Head of the Department, one senior faculty member and an external examiner. The external examiner shall be appointed by the Head of the Institution. For this, the Head of the department shall submit a panel of 3 examiners through Controller of Examinations. There are no internal marks for the comprehensive viva-voce and evaluated for maximum of 100 marks. A candidate has to secure a minimum of 50% of total marks to be declared successful. If he fails to fulfill minimum marks, he has to **reappear** during the supplementary examinations.

8.6 Evaluation of Project Work:

a) Every Student shall be required to execute his M.Tech. Project, under the guidance of the Supervisor assigned to him by the Head of the Department. The Project shall start immediately after the completion of the I Year II Semester, and shall continue through II Year I and II Semesters. The student shall carry out the literature survey, select an appropriate topic and submit a Project Proposal within 6 weeks (immediately after his I Year II Semester End Examinations), for approval by the Project Review Committee (PRC). The PRC shall be constituted by the Head of the Department, and shall consist of the Head of the Department, Project Supervisor, and two senior faculty members of the department. The student shall present his project work proposal to the PRC (PRC-I Presentation), on whose approval he can '**REGISTER** for the Project'. Every Student must compulsorily register for his M.Tech. Project Work, within the 6 weeks of time-frame as specified above. After registration, the student shall carry out his work, and continually submit 'a fortnightly progress report' to his Supervisor throughout the Project period. The PRC will monitor the progress of the project Work and review, through PRC-II and PRC-III Presentations – one at the end of the II Year I Semester, and one before the submission of M.Tech. project work report/ dissertation.

b) After PRC-III presentation, the PRC shall evaluate the entire performance of the Student and declare the Project Report as **'Satisfactory' or 'Unsatisfactory'**. Every Project Work Report/ Dissertation (that has been declared 'satisfactory') shall undergo **'Plagiarism Check'** as per the University/ College norms to ensure content plagiarism below a specified level of **30%**, and to become acceptable for submission. In case of unacceptable plagiarism levels, the student shall resubmit the project work report, after carrying out the necessary modifications/ additions to his project work/ report as per his Supervisor's advice, within the specified time, as suggested by the PRC.

c) If any student could not be present for PRC-II at the scheduled time (after approval and registration of his Project Work at PRC-I), his submission and presentation at the PRC-III time (or at any other PRC specified dates) may be treated as PRC-II performance evaluation, and delayed PRC-III dates for him may be considered as per PRC recommendations. Any Student is allowed to submit his MTech Project Dissertation **'only after completion of 40 weeks from the date of approval/registration'** of his Project, and after obtaining all approvals from the PRC.

d) After approval of project registration through PRC-I, a project work review-I will be conducted at the end of II year I semester for 100 marks through CIE only. Out of 100 marks the concernerd supervisor shall evaluate for 50 marks and remaining 50 marks by PRC-II. A candidate has to present and submit the project review-I report to the PRC-II. A candidate has to secure a minimum of 50% of total marks allotted. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

e) A project work review-II will be conducted at the end of II year II semester for 100 marks through CIE only. Out of 100 marks the concernerd supervisor shall evaluate for 50 marks and remaining 50 marks by PRC-III. A candidate has to present and submit the project review-II report to the PRC-III. A candidate has to secure a minimum of 50% of total marks allotted. If he fails to fulfill minimum marks, he has to reappear during the supplementary examination.

f) A total of 100 Marks are allotted for the M.Tech. Project Evaluation (Viva-Voce) SEE and there shall be no internal evaluation (CIE). The student shall be allowed to submit his Project Dissertation, only on the successful completion of all the prescribed M.Tech. Subjects (Theory and Labs.), Seminar, Comprehensive Viva-voce (securing B Grade or above), and after obtaining all approvals from PRC successfully. In such cases the M.Tech. dissertation will be sent to an External Examiner nominated by the Principal of the college, on whose 'approval', the student can appear for the M.Tech. Project Viva-voce Examination, which shall be conducted by **exam panel**, consisting of the project supervisor, Head of the Department and the External Examiner who adjudicated the Project Work and Dissertation. The **exam panel** shall jointly evaluate the performance for 100 Marks (SEE).

g) If the adjudication report of the External Examiner is **'not favourable'**, then the student shall revise and resubmit his Dissertation as per the time specified by the PRC. If the resubmitted report is again evaluated by the External Examiner as **'not favourable'**, then that Dissertation will be summarily rejected. Subsequent actions for such Dissertations may be considered, only on the specific recommendations of the PRC.

h) In cases, where the **exam panel** declared the Project Work Performance as **'unsatisfactory'**, the student is deemed to have failed in the Project Viva-voce Examination, and he has to **reappear** for the Viva-voce Examination as per the **exam panel** recommendations. If he fails in the second Viva-voce Examination also, he will not be considered eligible for the Award of the Degree, unless he is asked to revise and resubmit his Project Work by the **exam panel** in a specified time (within 4 years from the date of commencement of his I Year I Semester).

9. GRADING PROCEDURE

9.1 Marks will be awarded to indicate the performance of each student in each theory subject, lab/practical's, comprehensive viva-voce and project work. Based on the percentage of marks obtained in CIE+SEE (Continuous Internal Evaluation plus Semester End Examination), both taken together, as specified in item 10, and a corresponding letter grade shall be given.

9.2 As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades (UGC Guidelines) and corresponding percentage of marks shall be followed.

% of Marks Secured (Class Intervals)	Letter Grade (UGC Guidelines)	Grade Points
90% and above	O (Outstanding)	10
Below 90% but not less than 80%	A^+ (Excellent)	9
Below 80% but not less than 70%	A (Very Good)	8
Below 70% but not less than 60%	B^+ (Good)	7
Below 60% but not less than 50%	B (Average)	6
Below 50% (< 50%)	F (Fail)	0
Absent	**Ab**	**0**

9.3 A student obtaining F grade in any subject/course shall be considered '**failed**' and will be required to reappear as '**Supplementary Candidate'** in the Semester End Examination (SEE), as and when offered. In such cases, his internal marks (CIE Marks) in those subject(s) will remain same as those he obtained earlier.

9.4 A Letter Grade does not imply any specific % of marks.

9.5 In general, a student shall not be permitted to repeat any subject/course (s) only for the sake of '**Grade Improvement'** or '**SGPA/CGPA Improvement'**. However, he has to repeat all the subjects/courses pertaining to that semester, when he is detained.

9.6 A student earns **Grade Point** (GP) in each Subject/Course, on the basis of the letter grade obtained by him in that subject/course (excluding Mandatory non-credit courses). Then the corresponding '**Credit Points'** (CP) are computed by multiplying the grade point with credits for that particular subject/course.

Credit Points (CP) = Grade Point (GP) x Credits … For a Course

9.7 The Student passes the subject/course only when he gets GP ≥ 5 (B Grade or above).

9.8 The Semester Grade Point Average (SGPA) is calculated by dividing the sum of credit points (ΣCP) secured from **all** subjects/courses **registered** in a semester, by the total number of credits registered during that semester. SGPA is rounded off to **two** decimal places.

SGPA is thus computed as

$$SGPA = \{\sum_{i=1}^{N} C_i G_i\} / \{\sum_{i=1}^{N} C_i\} \quad \ldots \textbf{ for each semester},$$

where 'i' is the subject indicator index (takes into account all Subjects in a semester), **'N'** is the no. of subjects '**rigistered**' for the semester (as specifically required and listed under the course structure of the parent department), C_i is the no. of credits allotted to that i^{th} subject, and G_i represents the grade points (GP) corresponding to the letter grade awarded for that i^{th} subject.

9.9 The Cumulative Grade Point Average (CGPA) is a measure of the overall cumulative performance of a student over all semesters considered for registration. The CGPA is the ratio of the total credit Points secured by a student in **all** registered Courses in **all** semesters, and the total number of credits registered in **all** the semesters. CGPA is rounded off to **two** decimal places. CGPA is thus computed from the I year II semester onwards, at the end of each semester, as per the formula

$$CGPA = \{\sum_{j=1}^{M} C_j G_j\} / \{\sum_{j=1}^{M} C_j\} \quad \ldots \textbf{ for all S semesters registered}$$

(i.e., upto and inclusive of S semesters, S ≥ 2)

where **'M'** is the total number of subjects (as specifically required and listed under the course structure of the parent department) the Student has '**registered**' from the I year I semester onwards upto and inclusive of the semester S (obviously M > N), 'j' is the subject indicator index (takes into account all Subjects from 1 to S semesters), is the no. of credits allotted to the j^{th} subject, and represents the Grade Points (GP) corresponding to the letter grade awarded for that j^{th} subject. After registration and completion of I year I semester however, the SGPA of that semester itself may be taken as the CGPA, as there are no cumulative effects.

Illustration of calculation of SGPA					Illustration of calculation of CGPA			
Course /Subject	Credits	Letter Grade	Grade Points	Credit Points	Semester	Credits	SGPA	Credits x SGPA
Course 1	4	O	10	40	Sem I	28	7.00	196
Course 2	4	A^+	9	36	Sem II	28	6.00	168
Course 3	4	A	8	32	Sem III	16	6.50	104
Course 4	4	B^+	7	28	Sem IV	16	6.00	96
Course 5	4	B	6	24	Total	88		564
Course 6	4	F	0	0	CGPA=	6.41		
Total	24			160				
SGPA = 160/24 = 6.67								

9.10 For merit ranking or comparison purposes or any other listing, **only** the '**rounded off'** values of the CGPAs will be used.

9.11 For calculations listed in item 9.6 to 9.10, performance in failed subjects/courses (securing '**F'** grade) will also be taken into account, and the credits of such subjects/courses will also be included in the multiplications and summations.

10 PASSING STANDARDS:

10.1 A student shall be declared **'successful'** or **'passed'** in a semester, if student secures a GP ≥ 6.00 ('B' grade or above) in every subject/course in that semester (i.e. when student gets an SGPA ≥ 5.00 at the end of that particular semester); and a student shall be declared **'successful'** or **'passed'** in the entire post graduate programme, only when gets a CGPA ≥ 5.00 for the award of the degree as required.

10.2 After the completion of each semester, a '**Grade Card' or 'Grade Sheet'** (or **Transcript**) shall be issued to all the registered students of that semester, indicating the letter grades and credits earned. It will show the details of the courses registered (course code, title, number of credits, grade earned etc.), credits earned, SGPA, and CGPA.

10 DECLARATION OF RESULTS

11.1 Computation of SGPA and CGPA are done using the procedure in item Nos. 9.6 to 9.9.

11.2 For final percentage of marks equivalent to the computed final CGPA, the following formula may be used:

Percentage of Marks = (final CGPA – 0.5) x 10

12 AWARD OF DEGREE

12.1 After a student has satisfied the requirement prescribed for the completion of the Program and is eligible for the award of M.Tech. Degree he shall be placed in one of the following four classes based on CGPA:

Class Awarded	Grade to be Secured	Remarks
First Class with Distinction	≥ 8.00 CGPA	From the aggregate marks secured from 88 credits for regular students
First Class	≥ 6.50 to < 8.00 CGPA	
Second Class	≥ 5.50 to < 6.50 CGPA	
Pass Class	≥ 5.00 to < 5.50 CGPA	

12.2 First Class with Distinction will be awarded to those students who clear all the subjects in single attempt during his/her regular course of study by fulfilling the following conditions:

(i) Should have passed all the subjects/courses in '**first appearance'** within the first 2 academic years (or 4 sequential semesters) for M.Tech.

(ii) Should have secured a CGPA ≥8.00, at the end of each of the 4 sequential semesters.

(iii) Should not have been detained or prevented from writing the Semester End Examinations in any semester due to shortage of attendance or any other reason, shall be placed in '**First Class with Distinction'**.

12.3 **Award of Medals:** Students fulfilling the conditions listed under item 12.2 alone will be eligible for award of **'College ranks'** and **'Medals'**.

12.4 **Transcripts:** After successful completion of prerequisite credits for the award of degree a transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

13 WITH HOLDING OF RESULTS

If the student has not paid the fee to college at any stage, or has dues pending against his/her name due to any reason what so ever, or if any case of indiscipline is pending against him/her, the result of the student may be withheld, and he/she will not be allowed to go into the next higher semester. The award or issue of the degree may also be withheld in such cases.

14 SUPPLEMENTARY EXAMINATIONS

Supplementary examinations for odd semester subject(s) / course (s) shall be conducted along with even semester regular examinations and vice versa.

15. TRANSITORY REGULATIONS

a) **Re-Registration for Detained Students:** When any Student is detained in a Subject (s)/ Seminar due to shortage of attendance in any Semester, he may be permitted to re-register for the same Subject in the 'same category' (Core or Elective Group) or equivalent Subject if the same Subject is not available, as suggested by the Board of Studies of that Department, as when offered in the sub-sequent Semester(s), with the Academic Regulations of the Batch into which he seeks re-registration , with prior permission from the concerned authorities, subject to Item 3.0.

b) **Re-Admission for Discontinued Students:** Students, who have discontinued the M.Tech. Degree Programme due to any reasons what so ever, may be considered for 'Readmission' into the same Degree Programme (with same specialization) with the Academic Regulations of the Batch into which he gets readmitted, with prior permission from the concerned authorities, subject to Item 3.0.

c) A Student - who has discontinued for any reason, or who has been detained for want of attendance as specified, or who has failed after having undergone M.Tech. programme, may be considered eligible for readmission to the same programme with same set of Subjects/ Courses (or equivalent Subjects/ Courses as the case may be), and same Professional Electives (or from same set/category of Electives or equivalents as suggested), as and when they are offered (within the timeframe of 4 years from the Date of Commencement of his I Year I Semester).

16 STUDENT TRANSFERS: There shall be no transfers from other colleges/streams.

17 RULES OF DISCIPLINE

17.1 Any attempt by any student to influence the teachers, Examiners, faculty and staff of controller of Examination for undue favours in the exams, and bribing them either for marks or attendance will be treated as malpractice cases and the student can be debarred from the college.

17.2 When the student absents himself, he is treated as to have appeared and obtained zero marks in that subject(s) and grading is done accordingly.

17.3 When the performance of the student in any subject(s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject(s).

17.4 When the student's answer book is confiscated for any kind of attempted or suspected malpractice the decision of the Examiner is final.

18. MALPRACTICE

18.1 Malpractice Prevention Committee

A malpractice prevention committee shall be constituted to examine and punish the students who does malpractice / behaves indiscipline in examinations. The committee shall consist of:

a) Controller of Examinations - Chairman
b) Addl. Controller of Examinations.- Convener
c) Subject Expert - Member
d) Head of the Department of which the student belongs to - Member
e) The Invigilator concerned - Member

The committee shall conduct the meeting after taking explanation of the student and punishment will be awarded by following the malpractice rules meticulously.

Any action on the part of candidate at the examination like trying to get undue advantage in the performance at examinations or trying to help another, or derive the same through unfair means is punishable according to the provisions contained hereunder. The involvement of the Staff who are in charge of conducting examinations, valuing examination papers and preparing / keeping records of documents relating to the examinations, in such acts (inclusive of providing incorrect or misleading information) that infringe upon the course of natural justice to one and all concerned at the examination shall be viewed seriously and will be recommended for appropriate punishment after thorough enquiry.

18.2 Malpractice Rules: Disciplinary action for improper conduct in examinations

S. No.	Nature of Malpractices / Improper Conduct	Punishment
1 (a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination.	Expulsion from the examination hall and cancellation of the performance in that subject only.
1(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the Principal.
3	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred and forfeits the seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police

		and a case is registered against him.
4	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject.
6	Refuses to obey the orders of the Addl. Controller of examinations / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the addl. Controller of examinations or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the addl. Controller of examinations, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The candidates also are debarred and forfeit their seats. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course

		by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person(s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester/year examinations.
12	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the principal for further action to award suitable punishment.	

19. SCOPE

i) The academic regulations should be read as a whole, for the purpose of any interpretation.

ii) The above mentioned rules and regulations are applicable in general to M.Tech., unless and otherwise specific.

iii) In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Chairman of the Academic Council is final.

20. REVISION AND AMENDMENTS TO REGULATIONS

The Academic Council may revise or amend the academic regulations, course structure or syllabi at any time, and the changes or amendments made shall be applicable to all students with effect from the dates notified by the Academic Council Authorities.

COURSE STRUCTURE

CMR INSTITUTE OF TECHNOLOGY, HYDERABAD

(UGC AUTONOMOUS)

M.Tech. (VLSI SYSTEM DESIGN)

COURSE STRUCTURE

I Year – I Semester

	Course Title	Int. Marks	Ext. Marks	L	P	C
17EC1101CC	VLSI Technology	30	70	4	--	4
17EC1102CC	CMOS Analog Integrated Circuit Design	30	70	4	--	4
17 EC1103CC	CMOS Digital Integrated Circuit Design	30	70	4	--	4
17EC1104CE	Digital System Design Hardware Software Co Design CPLD and FPGA Architectures and Applications	30	70	4	--	4
17EC1105CE	Algorithms for VLSI Design Automation Embedded System Design Device Modeling	30	70	4	--	4
17EC1106OE	Soft Computing Techniques Image and Video processing Software Defined Radio	30	70	4	--	4
17EC1107CC	VLSI Laboratory – I	30	70	--	4	2
17EC1108CC	Seminar	100	--	--	4	2
	Total			**24**	**8**	**28**

I Year – II Semester

	Course Title	Int. Marks	Ext. Marks	L	P	C
17EC1201CC	Low Power VLSI Design	30	70	4	--	4
17 EC1202CC	Design for Testability	30	70	4	--	4
17EC 1203CC	CMOS Mixed Signal Circuit Design	30	70	4	--	4
17EC1204CE	VLSI and DSP Architectures Full Custom IC Design Hardware Description Language	30	70	4	--	4
17EC1205CE	Optimization Techniques in VLSI Design System On Chip Architecture Semiconductor Memory Design and Testing	30	70	4	--	4
17EC1206OE	Scripting Languages Theory and Techniques Adhoc Wireless Networks	30	70	4	--	4
17EC1207CC	VLSI Laboratory – II	30	70	--	4	2
17EC1208CC	Seminar	100	--	--	4	2
	Total			**24**	**8**	**28**

II Year - I Semester

	Course Title	Int. Marks	Ext. Marks	L	P	C
17EC2101CC	Comprehensive Viva-Voce	--	100	--	--	4
17EC2102CC	Project Work Review-I	100	--	--	24	12
	Total				**24**	**16**

II Year - II Semester

	Course Title	Int. Marks	Ext. Marks	L	P	C
17EC2201CC	Project Work Review-II	100	--	--	8	4
17EC2202CC	Project Evaluation (Viva-Voce)	--	100	--	16	12
	Total				**24**	**16**

M. Tech – I Year – I Sem. (VLSI System Design)

L	P	C
4	-	4

VLSI TECHNOLOGY

Course Objectives

1. To Understand the VLSI Technology and design of circuits based on technology like CMOS BICMOS etc
2. To Understand the designing layouts of logic gates
3. To learn descriptions and models of different processing steps involved in planar process starting from silicon crystal growth to packaging of circuits has to be dealt in depth.
4. To understand the processs of Diffusion and Chemical Vapour Deposition.
5. To provide in-depth knowledge of the Design Rules and Scaling of VLSI Circuits
6. To design VLSI circuits with technological process and design constraints.

Course Outcomes

1. Can design VLSI circuits starting from PMOS NMOS, CMOS, and BICMOS technology based design
2. Design the CMOS Circuit and Layout of logic gates on design tools
3. Understand the fundamentals behind integrated circuit design and manufacturing process.
4. Will acquire knowledge on oxidation, Lithography, Chemical vapour deposition and metallization.
5. Understand the basic principles of design rules and scaling standards.
6. Design VLSI circuits by keeping technological process constraints in mind

UNIT –I

Review of Microelectronics and Introduction to MOS Technologies:

MOS, CMOS, BiCMOS Technology. Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits: Ids – Vds relationships, Threshold Voltage VT, Gm, Gds and ωo, Pass Transistor, MOS, CMOS & Bi CMOS Inverters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT –II

Layout Design and Tools:

Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools. Logic Gates & **Layouts:**

Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and Inductive interconnect delays.

UNIT –III

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Yield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography, Doping and Depositions, Metallization. Ten step patterning process, Photo resists, physical properties of photo resists,

Storage and control of photo resists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT –IV

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitoxy, molecular beam epitaxy.

UNIT –V

Design rules and Scaling, BICMOS ICs: Choice of transistor types, pnp transistors, Resistors, capacitors,

Packaging: Chip characteristics, package functions, package operations

TEXT BOOKS

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000

REFERENCE BOOKS

1. Micro Electronics circuits Analysis and Design 2nd Edition, Muhammad H Rashid, CENAGE Learning2011.
2. Eugene D. Fabricius, Introduction to VLSI design, McGraw Hill, 1999
3. Wani-Kai Chen (editor), The VLSI Hand book, CRI/IEEE press, 2000
4. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994

M. Tech – I Year – I Sem. (VLSI System Design)

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CMOS ANALOG INTEGRATED CIRCUIT DESIGN

Course Objectives

1. To describe over view about evolution of CMOS integrated circuits.
2. To provide knowledge about fabrication process and technology of Analog CMOS Sub-Circuits and basic Current mirrors.
3. To introduce and familiarize with the various CMOS amplifier.
4. To introduce and familiarize with the various CMOS Operational Amplifiers.
5. To provide knowledge about different Comparators.
6. To prepare them to face the challenges in CMOS technology.

Course Outcomes

1. Develop an in-depth understanding of the design principles and applications of CMOS analog IC design.
2. An ability to know the fabrication steps involved in Analog CMOS Sub-Circuits and basic Current mirrors.
3. Familiar with the small signal and large signal models of CMOS Amplifiers.
4. Analyze and design of CMOS op-amps and compensation techniques.
5. Analyze and design of Comparators with Two-Stage, Open-Loop.
6. An ability to understand the basic concepts of CMOS technology and its simulation models.

UNIT -I

MOS Devices and Modeling:

The MOS Transistor, Passive Components- Capacitor & Resistor, Integrated circuit Layout, CMOS Device Modeling - Simple MOS Large-Signal Model, Other Model Parameters, Small-Signal Model for the MOS Transistor, Computer Simulation Models, Sub-threshold MOS Model.

UNIT -II

Analog CMOS Sub-Circuits:

MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT -III

CMOS Amplifiers:

Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT -IV

CMOS Operational Amplifiers:

Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT -V

Comparators:

Characterization of Comparator, Two-Stage, Open-Loop Comparators,Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

TEXT BOOKS

1. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
2. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition, 2010.

REFERENCE BOOKS

1. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edn, 2013. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition.
2. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.

M. Tech – I Year – I Sem. (VLSI System Design)

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CMOS DIGITAL INTEGRATED CIRCUIT DESIGN

Course Objectives

1. To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits, and Sequential MOS logic circuits.
2. To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.
3. To describe overview about CMOS integrated circuit.
4. To provide knowledge about combinational, sequential MOS logic circuits.
5. To understand the design of semiconductor memories.
6. To prepare them to face the challenges in dynamic logic circuits.

Course Outcomes

1. Student will able to understand the realization of different logic circuit designs for logic expressions.
2. Able to understand the importance of the circuit designs , the drawback of the designs both in combinational as well as sequential.
3. Able to know different types of memories , performance evaluation of each memory modules
4. Able to improve performance by taking different structures.
5. Able to know the design of semiconductor memories.
6. Able to design different combinational logic blocks.

UNIT –I

MOS Design:

Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT –II

Combinational MOS Logic Circuits:

MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates**.**

UNIT –III

Sequential MOS Logic Circuits:

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flipflop**.**

UNIT –IV

Dynamic Logic Circuits:

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT –V

Semiconductor Memories:

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

TEXT BOOKS

1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2nd Ed., PHI.

M. Tech – I Year – I Sem. (VLSI System Design)

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DIGITAL SYSTEM DESIGN
(Core Elective –I)

Course Objectives

1. To impart knowledge on the theory of Sequential machines and minimization of it.
2. to design digital circuits for various applications.
3. to learn fault diagnosis and testability algorithms
4. To learn digital design of Sequential Machines, drawing state graphs, realization and implementation of SM Charts.
5. To learn Fault modeling and test pattern generation of Combinational circuits.
6. To learn fault diagnosis in sequential circuits, machine design, identification of fault detection experiment.

Course Outcomes

1. Design digital circuits by their own for new applications.
2. Identify techniques to improve fault diagnosis for digital circuits.
3. Understand the design techniques of sequential Machines, and the fundamental concepts of PLD's, design of FPGA's.
4. Learn implementation of SM charts in combinational and sequential circuits.
5. Develop skills in modeling fault free combinational circuits and Develop skills in modeling Sequential circuits in terms of reliability, availability and safety.
6. Develop skills in modeling fault detection experiments of sequential circuits Develop skills in modelingcombinational circuits in terms of reliability, availability and safety.

UNIT -I

Minimization and Transformation of Sequential Machines:

The Finite State Model – Capabilities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races, Cycles and Hazards.

UNIT -II

Digital Design:

Digital Design Using ROMs, PALs and PLAs , BCD Adder, 32 – bit adder, State graphs for control circuits, Scoreboard and Controller, A shift and add multiplier, Array multiplier, Keypad Scanner, Binary divider.

UNIT -III

SM Charts:

State machine charts, Derivation of SM Charts, Realization of SM Chart, Implementation of Binary Multiplier, dice game controller.

UNIT -IV

Fault Modeling & Test Pattern Generation:

Logic Fault model – Fault detection & Redundancy- Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models –Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing, Transition count testing, Signature analysis and test bridging faults.

UNIT -V

Fault Diagnosis in Sequential Circuits:

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment, Machine identification, Design of fault detection experiment

TEXT BOOKS

1.Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.

2.Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

3.Logic Design Theory – N. N. Biswas, PHI

REFERENCE BOOKS

1. Switching and Finite Automata Theory – Z. Kohavi , 2nd Ed., 2001, TMH

2. Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI.

3. Digital Circuits and Logic Design – Samuel C. Lee , PHI

M. Tech – I Year – I Sem. (VLSI System Design)

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HARDWARE - SOFTWARE CO-DESIGN
(Core Elective –I)

Course Objectives

1. To design mixed hardware-software systems and the design of hardwaresoftware interfaces,
2. To focus on common underlying modeling concepts, and the trade-offs between hardware and software components
3. To learn about System –level specification, design representation for system level synthesis, system level specification languages
4. To Describe an embedded system design flow from specification to physical realization
5. To Describe structural behavior of systems, Master complex systems.
6. To Devise new theories, techniques, and tools in design, implementation and testing, and Master contemporary development techniques.

Course Outcomes

1. Able to design mixed hardware-software systems and the design of hardware-software interfaces
2. Able to focus on common underlying modeling concepts, , and the trade-offs between hardware and software components.
3. Able to learn about System –level specification, design representation for system level synthesis, system level specification languages.
4. Able to Gain knowledge of contemporary issues and algorithms used, and Know the interfacing components, different verification techniques and tools.
5. Able to Understand the use of modern hardware and software tools for building prototypes of embedded systems.
6. Able to Apply embedded software techniques to satisfy functional and response time requirements, Apply verification tools and Understand design representation for system level synthesis

UNIT –I

Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms:

Hardware software synthesis algorithms: hardware – software partitioning distributed system co- synthesis.

UNIT –II

Prototyping and Emulation:

Prototyping and emulation techniques, prototyping and emulation environments, future

developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures:

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT –III

Compilation Techniques and Tools for Embedded Processor Architectures:

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT –IV

Design Specification and Verification:

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification

UNIT –V

Languages for System – Level Specification and Design-I:

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II:

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS

1.Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – 2009, Springer.

2.Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami, 2002, Kluwer Academic Publishers

REFERENCE BOOKS

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont - 2010 – Springer

M. Tech – I Year – I Sem. (VLSI System Design)

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CPLD AND FPGA ARCHITECURES AND APPLICATIONS
(Core Elective –I)

Course objective

1. To understand the concept of programmable logic device architecture and technologies their basic structure.
2. To understand the architecture of the Altera MAX 7000 family of CPLDs
3. To understand the difference between CPLD and FPGA .
4. To provide knowledge about SRAM Programmable FPGA device architecture
5. To understand about Anti-Fuse Programmable FPGA architecture.
6. To provide knowledge about various applications of FPGA's.

Course outcomes

1. Learn important design practices to ensure the best and most stable CPLD & FPGA design
2. Learn the concepts of Programmable architectures
3. Ability to know about SRAM technology based FPGA's.
4. Ability to know about the Anti-Fuse Technology based FPGA's.
5. Ability to choose the appropriate FPGA architecture given a specific application.
6. Ability to construct a digital system using FPGA design.

UNIT-I

Introduction to Programmable Logic Devices:

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices – Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II

Field Programmable Gate Arrays:

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT -III

SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT -IV

Anti-Fuse Programmed FPGAs:

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT -V

Design Applications:

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.

REFERENCE BOOKS

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.
4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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ALGORITHMS FOR VLSI DESIGN AUTOMATION
(Core Elective –II)

Course Objectives

1. To understand the concepts and problems in Layout Compaction, Placement, Floorplanning And Routing
2. To know Logic Synthesis And Verification , High level Synthesis
3. To understand the Physical Design Automation of MCMs
4. To understand the Physical Design Automation of MCMs
5. To explain the various algorithms used to design VLSI in automation.
6. To study the various optimization techniques in the process of automation.

Course Outcomes

1. Able to understand the concepts and problems in Layout Compaction, Placement, Floorplanning And Routing
2. Able to know Logic Synthesis And Verification , High level Synthesis
3. Able to understand the Physical Design Automation of MCMs
4. Able to understand the Physical Design Automation of MCMs
5. Ability to model automation of VLSI design.
6. Ability to apply optimization techniques to the process of VLSI design.

UNIT I

PRELIMINARIES

Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

LAYOUT COMPACTION, PLACEMENT, FLOORPLANNING AND ROUTING

Problems, Concepts and Algorithms.

MODELLING AND SIMULATION

Gate Level Modelling and Simulation, Switch level Modelling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION

Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

HIGH-LEVEL SYNTHESIS

Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGAs

FPGA technologies, Physical Design cycle for FPGAs, partitioning and Routing for segmented and staggered Models.

PHYSICAL DESIGN AUTOMATION OF MCMs

MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCMs.

TEXT BOOKS

1. Algorithms for VLSI Design Automation, S.H.Gerez, 1999, WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd.
2. Algorithms for VLSI Physical Design Automation – Naveed Sherwani, 3rd Ed., 2005, Springer International Edition.

REFERENCE BOOKS

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, 1993, Wiley.
2. Modern VLSI Design:Systems on silicon – Wayne Wolf, 2nd ed., 1998, Pearson Education Asia.

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EMBEDDED SYSTEMS DESIGN
(Core Elective –II)

Course Objectives

1. To have knowledge about the basic functions of embedded systems
2. To know in detail about PIC microcontroller
3. To have knowledge about the basic structure of embedded systems
4. To discuss about the software environment in embedded systems
5. To learn about real time operating systems
6. To learn about task communication

Course Outcomes

1. Able to understand the concept of embedded systems
2. Able to know in detail about PIC microcontroller and interfacing
3. Able to understand in detail about embedded microcontroller and architecture
4. Able to apply software tools in various embedded hardware
5. Able to apply embedded system for real time applications
6. Able to understand task communication

UNIT -I

Introduction to Embedded Systems

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT -II

Typical Embedded System:

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

UNIT -III

Embedded Firmware:

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT -IV

RTOS Based Embedded System Design:

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT -V

Task Communication:

Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

TEXT BOOKS

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

REFERENCE BOOKS

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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DEVICE MODELLING
(Core Elective –II)

Course Objective

1. To impart to students knowledge of semi conductor physics and integrated passive devices.
2. To know about Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation ,
3. To learn about Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model dynamic model, Parasitic effects – SPICE model –Parameter extraction ,
4. To learn about An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS
5. To enable students to analyze the behavior of integrated NMOS and PMOS transistors with the help of SPICE models.
6. To enable students visualize different VLSI fabrication techniques of different processes and to model hetero junction devices.

Course Outcomes

1. Able to understand semi conductor physics and integrated passive devices.
2. Able to know about quantum mechanics, boltzman transport equation, continuity equation, poisson equation.
3. Able to understand types and structures in monolithic technologies – basic model (ebermoll) – gunmel - poon model dynamicmodel, parasitic effects – spice model – parameter extraction.
4. Able to understand an overview of wafer fabrication, wafer processing – oxidation – patterning
5. Able to analyze the behavior of integrated nmos and pmos transistors with the help of spice models.
6. Able to visualize different vlsi fabrication techniques of different processes and to model hetero junction devices.

UNIT -I

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, Continuity equation, Poisson equation. **Integrated Passive Devices:** Types and Structures of resistors and capacitors in monolithic technology, Dependence of model parameters on structures

UNIT -II

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – Static and Dynamic behavior – Small and large signal models – SPICE models **Integrated Bipolar**

Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) – Gunmel - Poon model- dynamic model, Parasitic effects – SPICE model –Parameter extraction

UNIT -III

Integrated MOS Transistor: NMOS and PMOS transistor – Threshold voltage – Threshold voltage equations – MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT –IV

VLSI Fabrication Techniques: An overview of wafer fabrication, Wafer Processing – Oxidation – Patterning – Diffusion – Ion Implantation – Deposition – Silicon gate nMOS process – CMOS processes – n-well- p-well- twin tub- Silicon on insulator – CMOS process enhancements – Interconnects circuit elements

UNIT -V

Modeling of Hetero Junction Devices: Band gap Engineering, Band gap Offset at abrupt Hetero Junction, Modified current continuity equations, Hetero Junction bipolar transistors (HBTs), SiGe **TEXT**

TEXT BOOKS

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid State Circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCE BOOKS

1. Physics of Semiconductor Devices – Sze S. M, 2nd Edition, Mcgraw Hill, New York, 1981.
2. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997.
3. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

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SOFT COMPUTING TECHNIQUES
(Open Elective - I)

Course Objective

1. To understand Fundamentals of Neural Networks & Feed Forward Networks
2. To understand basic concepts of Genetic Algorithm and its working principle
3. To know about Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule based systems
4. To know about Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perception, Adeline and Madeline, Feed-forward Multilayer Perceptron, Learning and Training the neural network,
5. To learn about fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling
6. To learn application of Neural networks and Fuzzy systems

Course Outcomes

1. Able to understand Fundamentals of Neural Networks & Feed Forward Networks
2. Able to understand basic concepts of Genetic Algorithm and its working principle
3. Able to Know about Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule based systems.
4. Able to Know about Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perception, Adeline and Madeline, Feedforward Multilayer Perceptron, Learning and Training the neural network.
5. Able to understand fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling
6. Able to understand application of Neural networks and Fuzzy systems

UNIT – I

Fundamentals of Neural Networks & Feed Forward Networks

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures, Signal Layer Feed Forward Neural Network :The Perceptron Model, Multilayer Feed Forward Neural Network :Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II

Associative Memories & ART Neural Networks

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks,

Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture.

UNIT – III

Fuzzy Logic & Systems

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT – IV

Genetic Algorithms

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT – V

Hybrid Systems

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

TEXT BOOKS

1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S.Rajasekaran, G.A. Vijayalakshmi Pai, July 2011, PHI, New Delhi.
3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.
4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

REFERENCE BOOKS

1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.
2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998
3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

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IMAGE AND VIDEO PROCESSING
(OPEN ELECTIVE-I)

Course Objectives

1. The student will be able to understand the quality of improvement methods of image.
2. To study the basic digital image and video filter operations and segmentation techniques.
3. To understand the fundamentals of image compression.
4. To Understand the representation video and video processing,interpolation techniques and standards.
5. To understand the principles and methods of motion estimation.
6. to implement image and videi processing algorithms and analyze and interpret the results of image processing methids and algorithms.

Course Outcomes

1. Understand digital imaging fundamentals will get working level knowledge on DCT, DFT, FFT on images.
2. Understand various image enhancement and segmentation techniques.
3. The students will learn image representation, filtering, compression.
4. Students will learn the basics of video processing, representation, interpolation.
5. Understand the video compression techniques and also learn about motion estimation.
6. Able to implement a complete image processing system to acheve a specific task, and analyze and interpret the results of this system.

UNIT –I

Fundamentals of Image Processing and Image Transforms:

Basic steps of Image Processing System Sampling and Quantization of an image, Basic relationship between pixels.

Image Segmentation: Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region based segmentation.

UNIT –II

Image Enhancement: Spatial domain methods:

Histogram processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, Image smoothing, Image sharpening, Selective filtering.

UNIT –III

Image Compression:

Image compression fundamentals - Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, Lossy Predictive coding, JPEG Standards.

UNIT -IV

Basic Steps of Video Processing:

Analog Video, Digital Video. Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT –V

Motion Estimation:

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS

1. Digital Image Processing – Gonzaleze and Woods, 3rd Ed., Pearson.
2. Video Processing and Communication – Yao Wang, Joem Ostermann and Ya–quin Zhang. 1st Ed., PH Int.

REFRENCE BOOKS

1. Digital Image Processing using MATLAB– Gonzaleze and Woods, 2nd ed., Mc Graw Hill Education, 2010
2. Image Processing Analysis , and Machine Vision- Milan Sonka, Vaclan Hlavac, 3 ed., CENGAGE, 2008
3. Digital Video Processing – A Murat Tekalp, PERSON, 2010
4. Digital Image Processing – S.Jayaraman, S.Esakkirajan, T.Veera Kumar –TMH, 2009

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SOFTWARE DEFINED RADIO
(Open Elective-I)

Course Objectives

1. To understand Characteristics and benefits of software radio
2. To understand Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure
3. To understand Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks
4. To understand Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals
5. To understand Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.
6. To understand JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT

Course Outcomes

1. Able to understand Characteristics and benefits of software radio
2. Able to understand Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure
3. Able to understand Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks
4. Able to understand Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals
5. Able to understand Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.
6. Able to understand JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT

UNIT -I

Introduction:

The Need for Software Radios, What is Software Radio, Characteristics and benefits of software radio- Design Principles of Software Radio, RF Implementation issues- The Purpose of RF Front – End, Dynamic Range- The Principal Challenge of Receiver Design – RF Receiver Front- End Topologies- Enhanced Flexibility of the RF Chain with Software Radios-

Importance of the Components to Overall Performance- Transmitter Architectures and Their Issues- Noise and Distortion in the RF Chain, ADC and DAC Distortion.

UNIT -II
Profile and Radio Resource Management :

Communication Profiles- Introduction, Communication Profiles, Terminal Profile, Service Profile , Network Profile, User Profile, Communication Profile Architecture, Profile Data Structure, XML Structure, Distribution of Profile Data, Access to Profile Data, Management of Communication Profiles, Communication Classmarks, Dynamic Classmarks for Reconfigurable Terminals, Compression and Coding, Meta Profile Data

UNIT -III
Radio Resource Management in Heterogeneous Networks:

Introduction, Definition of Radio Resource Management, Radio Resource Units over RRM Phases, RRM Challenges and Approaches, RRM Modelling and Investigation Approaches, Investigations of JRRM in Heterogeneous Networks, Measuring Gain in the Upper Bound Due to JRRM, Circuit- Switched System, Packet-Switched System, Functions and Principles of JRRM, General Architecture of JRRM, Detailed RRM Functions in Sub-Networks and Overall Systems

UNIT -IV
Reconfiguration of the Network Elements :

Introduction, Reconfiguration of Base Stations and Mobile Terminals, Abstract Modelling of Reconfigurable Devices, the Role of Local Intelligence in Reconfiguration, Performance Issues, Classification and Rating of Reconfigurable Hardware, Processing Elements, Connection Elements, Global Interconnect Networks, Hierarchical Interconnect Networks, Installing a New Configuration, Applying Reconfiguration Strategies, Reconfiguration Based on Comparison, Resource Recycling, Flexible Workload Management at the Physical Layer, Optimised Reconfiguration, Optimisation Parameters and Algorithms, Optimization Algorithms, Specific Reconfiguration Requirements, Reconfiguring Base Stations, Reconfiguring Mobile Terminals

UNIT -V
Object – Oriented Representation of Radios and Network Resources:
Networks- Object Oriented Programming- Object Brokers- Mobile Application Environments- Joint Tactical Radio System.

Case Studies in Software Radio Design:
Introduction and Historical Perspective, SPEAK easy- JTRS, Wireless Information Transfer System, SDR-3000 Digital Transceiver Subsystem, Spectrum Ware, CHARIOT.

TEXT BOOKS

1. Software Defined Radio Architecture System and Functions- Markus Dillinger, Kambiz Madani, WILEY 2003
2. Software Defined Radio: Enabling Technologies- Walter Tuttle Bee, 2002, Wiley Publications.

REFERENCE BOOKS

1. Software Radio: A Modern Approach to Radio Engineering - Jeffrey H. Reed, 2002, PEA Publication.
2. Software Defined Radio for 3G - Paul Burns, 2002, Artech House.
3. Software Defined Radio: Architectures, Systems and Functions - Markus Dillinger, Kambiz Madani, Nancy Alonistioti, 2003, Wiley.
4. Software Radio Architecture: Object Oriented Approaches to wireless System Enginering – Joseph Mitola, III, 2000, John Wiley & Sons.

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VLSI LABORATORY – I

Note:
Minimum of 10 programs from Part –I and 2 programs from Part -II are to be conducted.
Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools. The design shall include Gate-level design, Transistor-level design, Hierarchical design, Verilog HDL/VHDL design, Logic synthesis, Simulation and verification.

Course Objectives

1. To design combinational and sequential digital systems (Finite State Machines).
2. To understand the structural, register-transfer level (RTL), and algorithmic levels of abstraction for modeling digital hardware systems.
3. To understand and apply the concept of test-benches to create testing behavioral environments for simulation based verification.
4. To understand the design constraints during the implementation of the digital circuit on the FPGA .
5. To Design and Implement CMOS Transistor Level analog Circuits, Design a Schematic and Layout using Cadence tool
6. To study advanced features of verilog HDL and apply them to design complex real time digital systems and Implement them on the FPGA Boards.

Course Outcomes

1. Develop program codes for gate level and data flow modelling of combinational and sequential logic using Verilog HDL in any problem identification, formulation and solution.
2. Develop program codes for behavioral modelling of combinational and sequential logic using Verilog HDL in any problem identification, formulation and solution.
3. Design, simulate, and synthesize hardware using the Verilog hardware description language.
4. Design digital circuits with timing constraints on the FPGA Board
5. Design CMOS circuit Schematics and their Layouts in modern CAD tools
6. Develop a real time design on the FPGA/CPLD Boards.

Part –I: VLSI Front End Design programs:
Programming can be done using any complier. Down load the programs on FPGA/CPLD boards and performance testing may be done using pattern generator (32 channels) and logic analyzer apart from verification by simulation with any of the front end tools.

1. HDL code to realize all the logic gates
2. Design and Simulation of adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder.
3. Design of 2-to-4 decoder

4. Design of 8-to-3 encoder (without and with parity)
5. Design of 8-to-1 multiplexer
6. Design of 4 bit binary to gray converter
7. Design of Multiplexer/ Demultiplexer, comparator
8. Design of Full adder using 3 modeling styles
9. Design of flip flops: SR, D, JK, T
10. Design of 4-bit binary, BCD counters (synchronous/ asynchronous reset) or any sequence counter
11. Design of a N- bit Register of Serial- in Serial –out, Serial in parallel out, Parallel in Serial out and Parallel in Parallel Out.
12. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
13. Design of 4- Bit Multiplier, Divider.
14. Design of ALU to Perform – ADD, SUB, AND-OR, 1's and 2's Compliment, Multiplication, and Division.
15. Design of Finite State Machine.
16. Implementing the above designs on Xilinx/Altera/Cypress/equivalent based FPGA/CPLD kits.

Part –II: VLSI Back End Design programs:

Design and implementation of the following CMOS digital/analog circuits using Cadence / Mentor Graphics / Synopsys/Equivalent CAD tools. The design shall include Gate-level design/Transistor- level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - Basic logic gates
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS 1-bit full adder
   - Static / Dynamic logic circuit (register cell)
   - Latch
   - Pass transistor

Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths

M. Tech – I Year – II Sem. (VLSI System Design)

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LOW POWER VLSI DESIGN

Course Objectives

1. To know the sources of power consumption and need in CMOS circuits
2. To understand the fundamentals of low power circuit design and various power reduction techniques.
3. To study the design concepts of low power circuits and it's approaches.
4. To study and develop different logic styles using low power techniques.
5. To study and develop the concepts on different levels of optimization techniques of mulitpliers and adders
6. To study and develop knowledge of various power memories

Course Outcomes

1. Develops the basic fundamentals in low power design as reduction of power is much needed to enhance the performance of the system
2. Understand about the various low power VLSI design Techniques
3. Know the basics and advanced techniques in Low Power logic styles .
4. Understand and will be able to develop the capability of designing low power data path such as multipliers and adders
5. Understand about the design of low power memories for a VLSI system
6. Students will be able to design low power circuits

UNIT –I

Fundamentals:

Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT –II

Low-Power Design Approaches:

Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches.

Switched Capacitance Minimization Approaches:

System Level Measures, Circuit Level Measures, Mask level Measures.

UNIT –III

Low-Voltage Low-Power Adders:

Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques

–Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT –IV

Low-Voltage Low-Power Multipliers:

Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh- Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier.

UNIT –V

Low-Voltage Low-Power Memories:

Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXT BOOKS

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

REFERENCE BOOKS

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.
4. Practical Low Power Digital VLSI Design – Gary K. Yeap, Kluwer Academic Press, 2002.
5. Low Power CMOS VLSI Circuit Design – A. Bellamour, M. I. Elamasri, Kluwer Academic Press, 1995.
6. Leakage in Nanometer CMOS Technologies – Siva G. Narendran, AnathaChandrakasan, Springer, 2005.

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DESIGN FOR TESTABILITY

Course Objectives

1. To provide an introductory text on testability of Digital ASIC devices.
2. To introduce the student to various techniques which are designed to reduce the amount of input test patterns required to ensure that an acceptable level of Fault coverage has been obtained.
3. To design a workable system solution for a given problem is only half the Battle unfortunately
4. To introduce Simulation for Design Verification and Test Evaluation and Modeling Circuits for Simulation.
5. To design Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.
6. To know BIST Process, Pattern Generation, Response Compaction, and Built-In Logic Block Observers

Course Outcomes

1. Able to design complex digital systems using VLSI design meth
2. Able to design a digital system using given specifications and design constraints.
3. Able to assess logic and technology-septic parameters to control the functionality, system synchronization, power consumption, and Effects of circuit parasitic.
4. Able to design a significant VLSI design project having a set of objective criteria and design constraints
5. Able to design Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.
6. Able to know BIST Process, Pattern Generation, Response Compaction, and Built-In Logic Block Observers

UNIT -I

Introduction to Testing:

Testing Philosophy, Role of Testing, Digital and Analog VLSI Testing, VLSI Technology Trends affecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing, Levels of Fault Models, Single Stuck-at Fault.

UNIT -II

Logic and Fault Simulation:

Simulation for Design Verification and Test Evaluation, Modeling Circuits for Simulation, Algorithms for True-value Simulation, Algorithms for Fault Simulation, ATPG.

UNIT -III

Testability Measures:

SCOAP Controllability and Observability, High Level Testability Measures, Digital DFT and Scan Design: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan.

UNIT -IV

Built-In Self-Test:

The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, Response Compaction, Built-In Logic Block Observers, Test-Per-Clock, Test-Per-Scan BIST Systems, Circular Self Test Path System, Memory BIST, Delay Fault BIST.

UNIT -V

Boundary Scan Standard:

Motivation, System Configuration with Boundary Scan: TAP Controller and Port, Boundary Scan Test Instructions, Pin Constraints of the Standard, Boundary Scan Description Language: BDSL Description Components, Pin Descriptions.

TEXT BOOK

1. Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits - M.L. Bushnell, V.D. Agrawal, Kluwer Academic Pulishers.

REFERENCE BOOKS

1. Digital Systems and Testable Design - M. Abramovici, M.A.Breuer and A.D Friedman, Jaico Publishing House.
2. Digital Circuits Testing and Testability - P.K. Lala, Academic Press.

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CMOS MIXED SIGNAL CIRCUIT DESIGN

Course Objectives

1. To provide the concepts of switched capacitor circuits used in mixed signal circuit design.
2. To understand the design of Phase Locked Loop and Acquisition process using PLL.
3. To understand the dynamic specifications of D/A Converters.
4. To acquire knowledge on design different architectures of A/D Converters in mixed signal mode.
5. To gain knowledge on noise shaping modulators and higher order modulators and Biquad Filters.
6. To design mixed Signal Circuits using CMOS in State of Art CAD Tools

Course Outcomes

1. Analyze and design of switched capacitor circuits used in mixed signal circuit design
2. Demonstrate in-depth knowledge in PLL
3. Apply appropriate techniques, resources to engineering activities in development of D/A Converter
4. Solve engineering problems with wide range of solutions to increase data rate of A/D Converter
5. Design noise shaping converters given a set of requirements such as bandwidth, clock speed and signal-to-noise ratio
6. Design an integrated mixed signal circuit in CMOS using modern design tools •

UNIT -I

Switched Capacitor Circuits:

Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, biquad filters.

UNIT -II

Phased Lock Loop (PLL):

Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

UNIT -III

Data Converter Fundamentals:

DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

UNIT -IV

Nyquist Rate A/D Converters:

Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

UNIT -V

Oversampling Converters:

Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

TEXT BOOKS

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002
2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. Analog Integrated Circuit Design- David A. Johns,Ken Martin, Wiley Student Edition, 2013

REFERENCE BOOKS

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.
3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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VLSI AND DSP ARCHITECTURES
(Core Elective –III)

Course Objectives

1. To expose the students to the concept of pipeline and parallel processing in VLSI
2. To provide knowledge of realization of DSP system in VLSI.
3. To train students to understand DSP algorithms Cook-Toom Algorithm,Fast Convolution algorithm by Inspection.
4. To enable students to choose different parallelprocessing and pipeline processing techniques.
5. To train students to know about minimization techniques.
6. To enable students to Systolic Design for SpaceRepresentations contain Delays and to train students towards Power Reduction techniques and Power Estimation techniques.

Course Outcomes

1. Students will be able to design DSP system in VLSI.
2. Students will be able to design low power systems.
3. Students will be able to understand DSP algorithms Cook-Toom Algorithm,Fast Convolution algorithm by Inspection method.
4. Students will be able to choose different parallelprocessing and pipeline processing techniques.
5. Students will be able to understand minimization techniques.
6. Students will be able toknow Systolic Design for SpaceRepresentations contain Delays and know Power Reduction techniques and Power Estimation techniques

UNIT I

Essential feature of Instruction set architectures of CISC, RISC and DSP processors and their implications for implementation as VLSI Chips, Micro programming approaches for implementation of control part of the processor. Assessing understanding performance, Introduction, CPU performance and its factors, evaluating performance, real stuff: Two spec bench marks and performance of recent INTEL processors, fallacies and pitfalls

UNIT II

Data Path and Control: Introduction, logic design conventions, building a data path, a simple implementation scheme, a multi cycle implementation, exceptions, micro programming: simplifying control design, an introduction to digital design using hardware description language, fallacies and pitfalls

UNIT III

Enhancing performance with pipeline: An overview of pipelining, a pipe lined data path. Pipe lined control, data hazards and forwarding, data hazards and stalls, branch hazards using a

hard ware description language to describe and model a pipe line, exceptions, advanced pipelining: extracting more performance, fallacies and pitfalls

UNIT IV

Computational Accuracy in DSP implementations: Introduction, number formats for signals and coefficients in DSP system, dynamic range and precision, sources of errors in DSP implementations, A/D conversion errors, DSP computational errors, D /A conversion errors

UNIT V

Architectures for programmable digital signal processing devices: introduction, basic architectural features, DSP Computational building blocks, bus architecture and memory, data addressing capabilities, address generation unit, programmability and program execution, speed issues, features for external interfacing.

TEXT BOOKS

1. Computer Organization and Design: Hard ware/ Software Interface-D.A, Patterson and J.L Hennessy, 4th ed., Elsevier, 2011
2. Structural Computer organization, A.S Tannenbaum, 4th ed., Prentice-Hall, 1999

REFERENCE BOOKS

1. W. Wolf, Modern VLSI Design: System on Silicon, 2nd Ed., Person Education,1998
2. Keshab Parhi, VLSI Digital Signal Processing system design and implementations, Wiley 1999
3. Avatar sign, Srinivasan S, Digital Signal Processing implementations using DSP microprocessors with examples, Thomson 4th reprint, 2004.

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FULL CUSTOM DESIGN
(Core Elective –III)

Course Objectives

1 To understand CMOS VLSI manufacturing processes, Process design rules Significance of full custom IC design, layout design flows
2. To understand Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals
3. To understand Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics
4. To understand Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects
5. To understand Proper layout CAD tools for layout, Planning tools
6. To understand Layout generation tools, Support tools

Course Outcomes

1. Able to understand CMOS VLSI manufacturing processes, Process design rules Significance of full custom IC design, layout design flows
2. Able to understand Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals
3. Able to understand Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics
4. Able to understand Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects
5. Able to understand Proper layout CAD tools for layout, Planning tools
6. Able to understand Layout generation tools, Support tools

UNIT I

Introduction: Schematic fundamentals, Layout design, Introduction to CMOS VLSI manufacturing processes, Layers and connectivity, Process design rules Significance of full custom IC design, layout design flows.

UNIT II

Advanced techniques for specialized building blocks Standard cell libraries, Pad cells and Laser fuse cells, Advanced techniques for building blocks, Power grid Clock signals and

UNIT III

Interconnect routing. Interconnect layout design, Special electrical requirements, Layout design techniques to address electrical characteristics.

UNIT IV

Layout considerations due to process constraints Large metal via implementations, Step coverage rules, Special design rules, Latch-up and Guard rings, Constructing the pad ring, Minimizing Stress effects.

UNIT V

Proper layout CAD tools for layout, Planning tools, Layout generation tools, Support tools.

TEXT BOOKS

1. CMOS IC Layout Concepts Methodologies and Tools, Dan Clein, Newnes, 2000.
2. The Art of Analog Layout, 2nd Edition, Ray Alan Hastings, Prentice Hall, 2006.

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HARDWARE DESCRIPTION LANGUAGE
(Core Elective –III)

Course Objectives

1. To understand the design flow of the VLSI circuits with modern EDA tools.
2. To understand concurrent statements and sequential statements to design digital circuits.
3. To understand different styles of designing State Machines and Encoding Styles.
4. To understand ASM and mixed signal simulators.
5. To understand the language references.
6. To understand advanced features of HDL and apply them to design complex real time systems.

Course Outcomes

1. Will be familiar with the constructs and conventions of VHDL programming in EDA tools.
2. Design combinational and sequential logic circuits using behavioral models of VHDL.
3. Able to design different styles of state machines and encoding styles.
4. Model analog circuits using Verilog AMS.
5. Able to design different language references.
6. Able to design, simulate and synthesize the real time applications using VHDL.

UNIT I

Introduction: About VHDL, Design Flows & EDA Tools, Code Structure, Data types, Operators and Attributes: Operators, Attributes, User-Defined Attributes, Operator, overloading

UNIT II

Concurrent Code: Concurrent versus Sequential, Using Operators, WHEN, Generate and Block, Sequential Code: Process, Signals and Variables, IF, WAIT, CASE, Using Sequential, Code To Design Combinational Circuits

UNIT III

State Machines: Introduction, Design Style #1, Design Style #2 (Stored Output), Encoding Style: From Binary to OneHot

UNIT IV

Introduction to Verilog-AMS: Verilog Family of Languages, Mixed Signal Simulators, Applications of Verilog-AMS, Analog Modeling.

UNIT V

Language Reference: Basics, Data Types, Signals, Expressions, Analog Behavior

TEXT BOOKS

1. Circuit Design and Simulation with VHDL, Volnei A. Pedroni, 2nd Edition, MIT Press, 2010.
2. Designers Guide to Verilog AMS, Kenneth S Kundert, Olaf Zinke, Springer, 2004.

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OPTIMIZATION TECHNIQUES IN VLSI DESIGN
(Core Elective –IV)

Course Objective

1. To understand Statistical Modeling such as Process variation modeling, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling.
2. To Learn about Statistical timing analysis, parameter space techniques, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation
3. To Learn About GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA For VLSI Design,
4. To understand Layout And Test Automation, Partitioning-Automatic Placement, Routing Technology, Mapping For FPGA- Automatic Test Generation- Partitioning Algorithm,
5. To Learn Global Routing-FPGA Technology Mapping-Circuit Generation-Test Generation In A GA Frame Work
6. To understand Test Generation Procedures, Power Estimation-Application Of GA-Standard Cell Placement

Course Outcomes

1. Able to understand Statistical Modeling such as Process variation modeling, Principle component based modeling, Quad tree based modeling, Performance modeling-Response surface methodology, delay modeling.
2. Able to Learn about Statistical timing analysis, parameter space techniques, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation
3. Able to Learn About GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA For VLSI Design,
4. Able to understand Layout And Test Automation, Partitioning-Automatic Placement, Routing Technology, Mapping For FPGA- Automatic Test Generation- Partitioning Algorithm,
5. Able to Learn Global Routing-FPGA Technology Mapping-Circuit Generation-Test Generation In A GA Frame Work
6. Able to understand Test Generation Procedures, Power Estimation-Application Of GA-Standard Cell Placement

UNIT –I

Statistical Modeling:

Modeling sources of variations, Monte Carlo techniques, Process variation modeling-Pelgrom‟s model, Principle component based modeling, Quad tree based modeling,

Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT –II

Statistical Performance, Power and Yield Analysis

Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT –III

Convex Optimization:

Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Posynomial fitting.

UNIT –IV

Genetic Algorithm:

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-encoding-local improvement-WDFR Comparison of CAS-Standard cell placement-GASP algorithm-unified algorithm.

UNIT –V

GA Routing Procedures and Power Estimation:

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA-Standard cell placement-GA for ATG- problem encoding- fitness function-GA Vs Conventional algorithm.

TEXT BOOKS

1. Statistical Analysis and Optimization for VLSI: Timing and Power - Ashish Srivastava, Dennis Sylvester, David Blaauw, Springer, 2005.
2. Genetic Algorithm for VLSI Design, Layout and Test Automation - Pinaki Mazumder, E.Mrudnick, Prentice Hall,1998.
3. Convex Optimization - Stephen Boyd, Lieven Vandenberghe, Cambridge University Press, 2004.

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SYSTEM ON CHIP ARCHITECTURE
(Core Elective –IV)

Course Objectives

1. Instruction to system approach deals with how system assembled with the components, which components are involved in the system integration.
2. To introduce hardware and software programmability verses performance
3. To know about entire memory organization, starch pads, cache memories and objective in cache data how to deal the write polices
4. To describe system design approach with respect to the hardware and software
5. To analyze and choose from different reconfigurable devices for a system on chip
6. To know SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Course Outcomes

1. Able to know about how the system forms with the lot of component and has majority about system level interconnections .
2. Students will be acquired with the analytical skill to decide what type of processor is required to design an SOC for the undersigned application.
3. Able to know interconnect architectures and basic bus architectures.
4. Able to know SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.
5. Able to know Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling.
6. Able to analyze and choose from different reconfigurable devices for a system on chip

UNIT –I
Introduction to the System Approach:

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT –II
Processors:

Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III

Memory Design for SOC:

Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV

Interconnect Customization and Configuration:

Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –V

Application Studies / Case Studies:

SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

TEXT BOOKS

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

REFERENCE BOOKS

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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SEMICONDUCTOR MEMORY DESIGN AND TESTING
(Core Elective –IV)

Course Objectives

1. To understand Random Access Memory Technologies such as SRAM, MOS SRAM, SOI technology, CMOS DRAM, BICMOS DRAM
2. To understand Non-volatile Memoriessuch as Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories
3. To understand Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance
4. To understand Semiconductor Memory Reliability and Radiation Effects
5. To understand Advanced Memory Technologies and High-density Memory Packing Technologies
6. To understand Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

Course Outcomes

1. Able to understand Random Access Memory Technologies such as SRAM, MOS SRAM, SOI technology, CMOS DRAM, BICMOS DRAM
2. Able to understand Non-volatile Memoriessuch as Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories
3. Able to understand Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance
4. Able to understand Semiconductor Memory Reliability and Radiation Effects
5. Able to understand Advanced Memory Technologies and High-density Memory Packing Technologies
6. Able to understand Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

UNIT -I

Random Access Memory Technologies:

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS

DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

UNIT -II

Non-volatile Memories:

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT -III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT -IV

Semiconductor Memory Reliability and Radiation Effects:

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT -V

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions

TEXT BOOKS

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed., Prentice Hall.

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SCRIPTING LANGUAGES
(Open Elective-II)

Course Objectives

1. To understand Characteristics and uses of scripting languages
2. To understand PERL, Advanced PERL
3. To understand The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes
4. To understand Advanced TCL such as The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code
5. To understand Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK
6. To understand JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan., Object Oriented Programming Concepts

Course Outcomes

1. Able to understand Characteristics and uses of scripting languages
2. Able to understand PERL, Advanced PERL
3. To understand The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes
4. Able to understand Advanced TCL such as The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code
5. Able to understand Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-TK
6. Able to understand JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan., Object Oriented Programming Concepts

UNIT -I

Introduction to Scripts and Scripting:

Characteristics and uses of scripting languages, Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT -II

Advanced PERL:

Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT -III

TCL:

The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT -IV

Advanced TCL:

The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, running untrusted code, The C interface.

UNIT -V

TK and JavaScript:

Visual tool kits, Fundamental concepts of TK, TK by example, Events and bindings, Geometry managers, PERL-**TK.**

JavaScript – Object models, Design Philosophy, Versions of JavaScript, The Java Script core language, Basic concepts of Pythan.

Object Oriented Programming Concepts (Qualitative Concepts Only): Objects, Classes, Encapsulation, Data Hierarchy.

TEXT BOOKS

1. The World of Scripting Languages- David Barron, Wiley Student Edition, 2010.
2. Practical Programming in Tcl and Tk - Brent Welch, Ken Jones and Jeff Hobbs., Fourth edition.
3. Java the Complete Reference - Herbert Schildt, 7th Edition, TMH.

REFERENCE BOOKS

1. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann SerieS.
2. Tcl and the Tk Toolkit- John Ousterhout, 2nd Edition, 2009, Kindel Edition.
3. Tcl 8.5 Network Programming book- Wojciech Kocjan and Piotr Beltowski, Packt Publishing.
4. Tcl/Tk 8.5 Programming Cookbook- Bert Wheeler

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CODING THEORY AND TECHNIQUES
(Open Elective-II)

Course Objective

1. To Understand Coding for Reliable Digital Transmission and storage
2. To Understand Cyclic codes
3. To Understand Convolutional Codes
4. To Understand Turbo Codes, LDPC Codes
5. To Understand Space-Time Codes
6. To Understand Spatial Multiplexing

Course Outcomes

1. Able to Understand Coding for Reliable Digital Transmission and storage
2. Able to Understand Cyclic codes
3. Able to Understand Convolutional Codes
4. Able to Understand Turbo Codes, LDPC Codes
5. Able to Understand Space-Time Codes
6. Able to Understand Spatial Multiplexing

UNIT – I

Coding for Reliable Digital Transmission and storage

Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system

UNIT - II

Cyclic Codes : Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

UNIT – III

Convolutional Codes : Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

UNIT – IV

Turbo Codes

LDPC Codes- Codes based on sparse graphs, Decoding for binary erasure channel, Log-likelihood algebra, Brief propagation, Product codes, Iterative decoding of product codes, Concatenated convolutional codes- Parallel concatenation, The UMTS Turbo code, Serial concatenation, Parallel concatenation, Turbo decoding

UNIT - V

Space-Time Codes

Introduction, Digital modulation schemes, Diversity, Orthogonal space- Time Block codes, Alamouti's schemes, Extension to more than Two Transmit Antennas, Simulation Results, Spatial Multiplexing : General Concept, Iterative APP Preprocessing and Per-layer Decoding, Linear Multilayer Detection, Original BLAST Detection, QL Decomposition and Interface Cancellation, Performance of Multi – Layer Detection Schemes, Unified Description by Linear Dispersion Codes.

TEXT BOOKS

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice Hall, Inc.
2. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill

REFERENCE BOOKS

1. Error Correcting Coding Theory-Man Young Rhee-1989,McGraw – Hill Publishing,19
2. Digital Communications-Fundamental and Application - Bernard Sklar, PE.
3. Digital Communications- John G. Proakis, 5th ed., 2008, TMH.
4. Introduction to Error Control Codes-Salvatore Gravano-oxford
5. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley India.
6. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Edition, 2009, TMH.

M. Tech – I Year – II Sem. (VLSI System Design)

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AD-HOC WIRELESS NETWORKS
(Open Elective-II)

Course Objectives

1. Understand need fundamentals of WLANs, IEEE802.11 standard and adhoc networks.
2. Explain the constraints of physical layer that effect the design and performance of adhoc network.
3. Understand why protocols required for wired network may not work for wired network at MAC, Network and transport layer.
4. Explain the operations and performance of various MAC layer protocols, unicast routing protocol and transport layer protocol proposed for adhoc networks.
5. Understand security issues and Qos requirements.
6. Understand need proactive routing protocol function and their implications on data transission delay and bandwidth consumption.

Course Outcomes

1. Understand the challenges in design of wireless adhoc networks and fundamentals of WLAN, IEEE802.11 standard.
2. Understand and analyze proposed protocols at MAC for adhoc wireless networks and issues in designing MAC protocol.
3. Learn about issues in designing a routing protocol and transport layer of adhoc networks.
4. Understand and analyze attacks pertaining to network layer.
5. Learn about security issues in adhoc networks and Qoa requirements.
6. Understanding how to proactive routing protocols function and their implications on data transmission delay and bandwidth consumption.

UNIT - I

Wireless Local Area Networks

Introduction, wireless LAN Topologies, Wireless LAN Requirements,Physical Layer-Infrared Physical Layer, Microwave based Physical Layer Alternatives, Medium Access Control Layer- HIPERLAN 1 Sublayer, IEEE 802.11 MAC Sublayer and Latest Developments-802.11a, 802.11b, 802.11g

Personal Area Networks: Introduction to PAN technology and Applications, Bluetooth - specifications, Radio Channel, Piconets and Scatternets, Inquiry, Paging and Link Establishment, Packet Format, Link Types, Power Management, Security, Home RF -Physical and MAC Layer

UNIT - II

MAC Protocols

Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that use Directional Antennas, Other MAC Protocols.

UNIT - III

Routing Protocols

Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

UNIT – IV

Transport Layer Protocols

Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other Transport Layer Protocol for Ad Hoc Wireless Networks.

UNIT – V

Quality of Service in Ad Hoc Wireless Networks:

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

TEXT BOOKS

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Networks -P Nicopolitidis and M S Obaidat, Wiley India Edition 2003.

REFERENCE BOOKS

1. Wireless Communication Technology- Roy Blake, CENGAGE,2012
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control - Jagannathan Sarangapani, CRC Press.

M. Tech – I Year – II Sem. (VLSI System Design)

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VLSI LABORATORY - II

Note: All the following digital/analog circuits are to be designed and implemented using Cadence / Mentor Graphics / Synopsys / Equivalent CAD tools.

The design shall include Gate-level design/Transistor-level design/Hierarchical design/Verilog HDL or VHDL design, Logic synthesis, Simulation and verification, Scaling of CMOS Inverter for different technologies, study of secondary effects (temperature, power supply and process corners), Circuit optimization with respect to area, performance and/or power, Layout, Extraction of parasitics and back annotation, modifications in circuit parameters and layout consumption, DC/transient analysis, Verification of layouts (DRC, LVS).

Course Objectives

1. To provide the practical design knowledge of VLSI circuits using CAD tools
2. To draw the schematic and layout of design using Cadence Virtuoso tool
3. To understand about SPICE simulation of basic analog circuits
4. To provide design capability of circuit at layout level and verification after extraction of parasitic
5. Exposure to various stages of a typical ‘state of the art’ CAD VLSI tool including the synthesis, place and route, layout, LVS, simulation, and power and clock routing modules
6. To design a layout for a system level design

Course Outcomes

1. Develops an ability to know the CAD tools to design VLSI circuits.
2. Develops an ability to draw the Layout of any combinational circuits.
3. Develop skills in SPICE simulation and Analog Circuit simulation
4. Simulate circuits within a CAD tool and compare to design specifications.
5. Analyze the results of logic and timing simulations and to use these simulation results to debug digital systems
6. Develops an ability to build the VLSI System level design.

VLSI Back End Design programs:

1. Introduction to layout design rules
2. Layout, physical verification, placement & route for complex design, static timing analysis, IR drop analysis and crosstalk analysis of the following:
   - CMOS inverter
   - CMOS NOR/ NAND gates
   - CMOS XOR and MUX gates
   - CMOS half adder and full adder
   - Static / Dynamic logic circuits (register cell)
   - Latch

- Pass transistor

3. Layout of any combinational circuit (complex CMOS logic gate)- Learning about data paths
4. Introduction to SPICE simulation and coding of NMOS/CMOS circuit
5. SPICE simulation of basic analog circuits: Inverter / Differential amplifier
6. Analog Circuit simulation (AC analysis) – CS & CD amplifier
7. System level design using PLL.